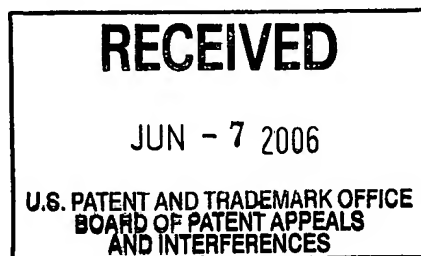


DOCKET NO. SC12865TH

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT Afzal Malik et al. GROUP ART UNIT: 2189
APPLN. NO.: 10/600,959 EXAMINER: Christian Chace
FILED: June 20, 2003 APPEAL No.: 2006-1007
TITLE: METHOD AND APPARATUS FOR DYNAMIC PREFETCH
BUFFER CONFIGURATION AND REPLACEMENT

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REQUEST FOR REHEARING UNDER 37 CFR 1.197

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

In a decision mailed May 31, 2006 the Board of Patent Appeals and Interferences did not sustain any of the examiner's rejections. However, in copying claim 1 on page 1 of the opinion, an inadvertent typographical error was placed into the recited claim 1. Applicants' Appeal Brief did not contain this error in claim 1. The file history of the application did not previously contain this error. Applicants request written correction of the opinion as a result of the typographical error.

In particular, on the last line of page 1 of the opinion, the word "positions" in claim 1 should be "portions". Applicants submit that this error was unrelated to the merits of the decision and request confirmation that this error did not affect the outcome of the Board's

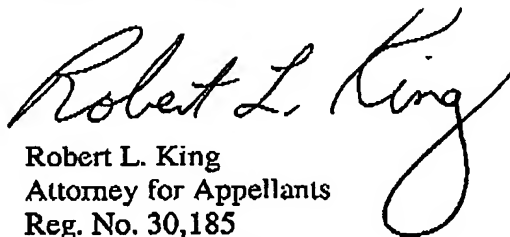
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decision. For referencce, Applicants are herein submitting the Claims Appendix as previously submitted in Applicants' Appeal Brief.

Appellants respectfully request confirmation of the same appeal decision result when the typographical error within claim 1 is acknowledged.

Respectfully submitted,
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Claims Appendix

1. (Previously Presented) A method for configuring a prefetch buffer, comprising:
receiving a read request from a master; and
in response to the read request, selectively modifying total length of one or more
prefetch buffer lines of the prefetch buffer based on an attribute of the read
request to an adjusted line size, thereby eliminating dedication of buffer
storage to unused portions of the one or more prefetch buffer lines, the
prefetch buffer having lines of differing total length during operation.
2. (Original) The method of claim 1, wherein the attribute of the read request comprises one
of a master identifier corresponding to the master, a data size of the read request, and a
burst length of the read request.
3. (Previously Presented) The method of claim 2, wherein selectively modifying the total
length of one or more prefetch buffer lines is based on a second attribute of the read
request, wherein the second attribute comprises another one of the master identifier, the
data size, and the burst length.
4. (Original) The method of claim 1, wherein the read request results in a miss in the prefetch
buffer.
5. (Original) The method of claim 1, wherein the prefetch buffer includes a plurality of lines,
each of the plurality of lines having a corresponding one of status fields.
6. (Original) The method of claim 5, further comprising:
selecting at least a portion of the plurality of lines as a replacement entry within
the prefetch buffer based on the status fields of the prefetch buffer.
7. (Original) The method of claim 6, wherein each of the status fields comprise an address tag
field, an invalid field to indicate that a corresponding line in the prefetch buffer is not valid,

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a used field to indicate that a corresponding line in the prefetch buffer has been provided in response to a previous burst read request, and a valid field to indicate a corresponding line in the prefetch buffer has been provided in response to a previous non-burst read request.

8. (Previously Presented) The method of claim 6, wherein selectively modifying the total length of one or more prefetch buffer lines comprises selectively modifying a line size of the replacement entry.
9. (Original) The method of claim 8, wherein selectively modifying the line size of the replacement entry comprises selectively modifying a status field corresponding to the replacement entry.
10. (Original) The method of claim 9, wherein selectively modifying the status field corresponding to the replacement entry is based on the attribute of the read request, the attribute comprising at least one of a data size and a burst length of the read request.

Claims 11 and 12 (Canceled)

13. (Original) The method of claim 10, further comprising:
 - generating at least one data request to a memory addressed by the read request;
 - and
 - storing data from the memory into the replacement entry of the prefetch buffer.
14. (Previously Presented) A method for configuring a prefetch buffer, comprising:
 - receiving a read request to a memory from a requesting master, the read request having a corresponding data size and burst length;
 - providing a prefetch buffer reconfiguration indicator based on the data size and the burst length;
 - selecting a replacement entry within the prefetch buffer;
 - based on the prefetch buffer reconfiguration indicator, selectively modifying total length of the replacement entry of the prefetch buffer based on an attribute

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of the read request to an adjusted line size that eliminates dedicating unused buffer storage to the replacement entry of the prefetch buffer; and storing data fetched from the memory in the replacement entry.

15. (Original) The method of claim 14, wherein the prefetch buffer reconfiguration indicator is based on the data size, the burst length, and a master identifier corresponding to the requesting master.
16. (Previously Presented) The method of claim 14, wherein selectively modifying the total length of the replacement entry comprises selectively modifying at least one status field corresponding to the replacement entry.
17. (Original) The method of claim 16, wherein the at least one status field comprises an address tag field, wherein selectively modifying the at least one status field comprises selectively modifying the address tag field.
18. (Original) The method of claim 14, wherein selecting the replacement entry within the prefetch buffer comprises checking at least one of valid, invalid, or used bits within status fields of the prefetch buffer.
19. (Original) The method of claim 14, further comprising:
 - generating at least one data fetch request to the memory, wherein the at least one data fetch request is based on a bus width corresponding to the memory.
20. (Allowed) A data processing system, comprising:
 - a master;
 - a memory;
 - a prefetch buffer, coupled to the master and the memory, the prefetch buffer having a plurality of lines and status fields, each of the plurality of lines having a corresponding one of the status fields, each of the status fields comprises an address tag field, an invalid field to indicate that a

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corresponding line in the prefetch buffer is not valid, a used field to indicate that a corresponding line in the prefetch buffer has been provided in response to a previous burst read request, and a valid field to indicate a corresponding line in the prefetch buffer has been provided in response to a previous non-burst read request; and

prefetch control circuitry coupled to the prefetch buffer, the prefetch control circuitry, in response to a read request from the master, selectively modifying a line size of at least a portion of the prefetch buffer.

21. (Allowed) The data processing system of claim 20, wherein the prefetch control circuitry selects a replacement entry within the prefetch buffer, and selectively modifying the line size comprises selectively modifying a line size of the replacement entry.
22. (Allowed) The data processing system of claim 21, wherein the prefetch control circuitry receives a data size indicator and a burst length indicator from the master and selectively modifies the line size of the replacement entry based on the data size indicator and the burst length indicator.

Claims 23 and 24 (Canceled)